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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,900 | WARE, FREDERICK A. | |
| | Examiner | Art Unit | |
| | Lev I. Iwashko | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/5/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 6-10, 13-22, 24, 26-27 and 30-32 are rejected under U.S.C. 102(b) as being anticipated by Olarig et al. (US Patent 6,260,127 B1).

Claim 1. A controller, comprising:

- a first memory interface adapted to be coupled to one or more first memory devices of a first memory type having a first set of attributes; a second memory interface adapted to be coupled to one or more second memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute; *(Column 2, lines 32-46 – State the following: "Briefly, the present invention describes, in one embodiment, a memory controller capable of supporting heterogeneous memory configurations. Several different memory module types are coupled to a bus via the memory controller of the present invention, and communications occur seamlessly with the bus. The memory controller receives memory requests from one or more processors or other bus masters via the bus. The memory controller receives the memory request, identifies a memory, and also memory access parameters, and accesses the memory and returns the resulting data (during a read request) or stores the data (during a write request). When the memory provides the data (on a read request), to*

*the memory controller, the memory controller provides the resulting data to the bus, where it can be read by the processor")*

- and interface logic coupled to the first and second interfaces and configured to direct memory transactions having a predefined first characteristic to the first memory interface and to direct memory transactions having a predefined second characteristic to the second memory interface. *(Column 12, lines 30-38 – State the following: "The multiplexer or selector 720 is controlled by a control logic and controller 730. The control logic and controller 730 receives a system geographic address 732 and a serial clock 734, according to the I.sup.2 C protocol. The control logic and controller 730 provides a three bit selection signal over a selection bus 734 to the multiplexer and selector 720. The three bit selection signal cycles through the eight DIMMs 702-716, passing each of the parallel presence detect values 550 to the eight bit parallel presence detect bus 722 in turn")*

Claim 2. The controller of claim 1, wherein the second memory devices are non-volatile memory devices. *(Column 5, lines 19-28 – State the following: "Devices that exchange data with the microprocessor typically are assigned I/O space allocations that may or may not be shared with other devices. Devices include memories, as well as peripheral and other devices. To encode the process of communicating with the devices in the system, the POST typically creates within non-volatile memory an allocation map, allowing a particular device to be identified by an identifier or handle of only a few bits, and a controller translate the handle into an identification of the corresponding resource and by I/O address")*

Claim 6. The controller of claim 1, further comprising: a write cache for storing data associated with write operations directed to any of the one or more second memory devices. *(Column 4, lines 30-35 – State the following: "Also coupled to the host bus 110 is a cache 104. The cache may be a*

*write through, a write back, or multi-level cache system for storing commonly used or recently used data values. The cache generally consists of a high-speed static RAM structure, addressable within the memory space of the processor's address lines")*

Claim 7. The controller of claim 6, wherein the write cache is configured to write data stored therein to the one or more second memory devices when a predefined write cache state occurs. *(Column 25, lines 9-13 – State the following: "The chunk order logic in the RPM is used to determine the order in which a 8-byte wide chunk of data (within a 32-byte or 64-byte wide cache line) is transferred onto memory data bus 370 on bus 310 when data is accessed over the memory bus 310")*

Claim 8. The controller of claim 6, wherein the controller is configurable to write data stored therein to the one or more second memory devices. *(Column 6, lines 29-30 – State the following: "For example, the memory controller 200 may be configured for a particular DRAM protocol")*

Claim 9. The controller of claim 6, wherein the controller is adapted to relocate one or more pages from the one or more second memory devices to the one or more first memory devices when a predefined write cache state occurs. *(Column 25, lines 9-13 – State the following: "The chunk order logic in the RPM is used to determine the order in which a 8-byte wide chunk of data (within a 32-byte or 64-byte wide cache line) is transferred onto memory data bus 370 on bus 310 when data is accessed over the memory bus 310")*

Claim 10. The controller of claim 1, wherein the one or more first memory devices are Dynamic Random Access Memory (DRAM) devices and the one or more second memory devices are Flash memory devices. *(Column 12, lines 44-47 – State the following: "Both the high address on bus 722 and the low address on bus 736 are provided to a 32 KB ROM 740 or other memory such as Flash, embedded DRAM or SRAM, containing the corresponding look up table")*

Claim 13. The controller of claim 1, wherein the memory controller is configurable to move pages from the one or more first memory devices to secondary storage and to then power down the one or more first memory devices. *(Column 24, lines 15-23 – State the following: "The internal hardware or firmware of the middle portion 304 of the RPM 300 performs memory address translation between the front end 302 and the back end 306; i.e., between a standard SDRAM protocol compatible with memory bus 210, (and also with memory module 240 and memory controller 200) and a device type protocol compatible with device 320 and memory bus 310. As stated previously, the memory module 320 may have one, two, or four physical memory modules there within")*

Claim 14. The controller of claim 1, wherein the controller is adapted for use in conjunction with a processor having virtual memory logic for mapping virtual memory addresses into physical memory addresses and page logic for assigning physical memory addresses to virtual memory addresses, wherein the page logic is configured to assigned physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and to assigned physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic. *(Column 25, lines 35-45 and Column 26, lines 1-3 and 23-45 – State the following: "Referring now to Tables 4, 5, and 6, the internal bit mapping within the memory personality module 300, implementing some of the translations in Table 2 and Table 3, are shown in greater detail. The first column 572 shows possible SDRAM DIMM sizes used on bus 210. The front end 302 is coupled to memory bus 210 using a protocol according to column 572. The protocol according to column 572 is compatible with memory bus 210, memory module 240, and memory controller 200. The second column of Tables 4, 5, and 6., i.e., column 690, shows the bit mapping within the memory personality module 300 when the back end*

*306 is coupled to a logical DIMM consisting of two physical EDO DIMMs". "Address translation for multiple physical memory modules within a logical memory is further illustrated by way of an example. As shown in the first row of Tables 4, two 8-megabyte EDO DIMMs may be used at the back end 306 of the memory personality module 300, having 12 bits of row address and 8 bits of column address, as shown in column 690'. The front end 302 is connected to memory bus 210 requiring 11 bits of row address, 9 bits of column address, and one bank select bit BA0. During the bank activate command phase, the lower eleven bits of memory address on address bus 352 of the front end 302 are directly mapped to the lower eleven bits of memory address on memory address bus 362 at the back end 306. Also, the bank select bit BA0 at the front end 302 is mapped to the bit RA11 of memory address on memory address bus 362 at the back end 306. Subsequently, during the read or write command phase, the address bits A8 to A1 on address bus 352 at the front end 302 are mapped to the address bits A7 to A0 on memory address bus 362 at the back end 306, while address bits A1 and A0 are mapped as inputs to a chunk order control circuit to control the order in which the data chunks are to be bursted to/from memory")*

Claim 15. The system, comprising: a first memory interface adapted to be coupled to one or more first memory devices of a first memory type having a first set of attributes; a second memory interface adapted to be coupled to one or more second memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute; interface logic coupled to the first and second interfaces and configured to direct memory transactions having a predefined first characteristic to the first memory interface and to direct memory transactions having a predefined second characteristic to the second memory interface; and a processor having virtual memory logic for mapping virtual memory addresses into physical memory addresses and

page logic for assigning physical memory addresses to virtual memory addresses, wherein the page logic is configured to assign physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and to assign physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic. *(Column 2, lines 32-46 – State the following: "Briefly, the present invention describes, in one embodiment, a memory controller capable of supporting heterogeneous memory configurations. Several different memory module types are coupled to a bus via the memory controller of the present invention, and communications occur seamlessly with the bus. The memory controller receives memory requests from one or more processors or other bus masters via the bus. The memory controller receives the memory request, identifies a memory, and also memory access parameters, and accesses the memory and returns the resulting data (during a read request) or stores the data (during a write request). When the memory provides the data (on a read request), to the memory controller, the memory controller provides the resulting data to the bus, where it can be read by the processor." Column 12, lines 30-38 – State the following: "The multiplexer or selector 720 is controlled by a control logic and controller 730. The control logic and controller 730 receives a system geographic address 732 and a serial clock 734, according to the I.sup.2 C protocol. The control logic and controller 730 provides a three bit selection signal over a selection bus 734 to the multiplexer and selector 720. The three bit selection signal cycles through the eight DIMMs 702-716, passing each of the parallel presence detect values 550 to the eight bit parallel presence detect bus 722 in turn." Column 25, lines 35-45 and Column 26, lines 1-3 and 23-45 – State the following: "Referring now to Tables 4, 5, and 6, the internal bit mapping within the memory personality module 300, implementing some of the translations in Table 2 and Table*

*3, are shown in greater detail. The first column 572 shows possible SDRAM DIMM sizes used on bus 210. The front end 302 is coupled to memory bus 210 using a protocol according to column 572. The protocol according to column 572 is compatible with memory bus 210, memory module 240, and memory controller 200. The second column of Tables 4, 5, and 6., i.e., column 690, shows the bit mapping within the memory personality module 300 when the back end 306 is coupled to a logical DIMM consisting of two physical EDO DIMMs". "Address translation for multiple physical memory modules within a logical memory is further illustrated by way of an example. As shown in the first row of Tables 4, two 8-megabyte EDO DIMMs may be used at the back end 306 of the memory personality module 300, having 12 bits of row address and 8 bits of column address, as shown in column 690'. The front end 302 is connected to memory bus 210 requiring 11 bits of row address, 9 bits of column address, and one bank select bit BA0. During the bank activate command phase, the lower eleven bits of memory address on address bus 352 of the front end 302 are directly mapped to the lower eleven bits of memory address on memory address bus 362 at the back end 306. Also, the bank select bit BA0 at the front end 302 is mapped to the bit RA11 of memory address on memory address bus 362 at the back end 306. Subsequently, during the read or write command phase, the address bits A8 to A1 on address bus 352 at the front end 302 are mapped to the address bits A7 to A0 on memory address bus 362 at the back end 306, while address bits A1 and A0 are mapped as inputs to a chunk order control circuit to control the order in which the data chunks are to be bursted to/from memory")*

Claim 16. The system of claim 15, wherein the first usage characteristic comprises memory usage that includes both read and write operations. *(Column 2, lines 39-43 – State the following: "The memory controller receives the memory request, identifies a memory, and also memory access*

*parameters, and accesses the memory and returns the resulting data (during a read request) or stores the data (during a write request)")*

Claim 17. The system of claim 16, wherein the second usage characteristic comprises memory usage that includes only read operations. *(Column 2, lines 43-46 – State the following: "When the memory provides the data (on a read request), to the memory controller, the memory controller provides the resulting data to the bus, where it can be read by the processor")*

Claim 18. The system of claim 16, wherein the second usage characteristic comprises memory usage that includes read operations and less than a threshold amount of write operations. *(Column 5, lines 50-67 and Column 6, lines 1-10 – State the following: "Upon detecting and receiving a pending memory request, the memory controller 200 decodes the request and provides an address and timing information to the bus 210. The memory controller 200 asserts the appropriate commands and other signals as needed. Often, the memory controller 200 stores several requests of the read type, or several requests of the write type to prevent having to reverse the memory bus 210 except as necessary. Because reversing the memory bus requires additional settling time, and because multiple read accesses or multiple write accesses can occur in rapid succession without having to reverse the memory bus 210, the memory controller 200 often groups memory access addresses. Also, paging is possible. Memory controller 200 typically provides a large number of functions, particularly in systems having multiple processors. For example, memory controller 200 receives and services tagged memory access requests from central processing unit 100 over host bus 110. When central processing unit 100 desires to read data from, or write data to, a memory module, the central processing unit 100 provides a memory access request to the host bus 110. The memory access request includes a tag and an address. On a write access, the request also includes data. The tag is an identifier or value that is unique among requests that are currently pending on the host bus*

*110. The memory controller 200 services pending requests by accessing memory to read data from, or write data to, a memory location within the memory (DRAM 102) corresponding to the address. When the access request is a write request, the memory controller 200 provides the data (and a write command) over memory bus 310 to a memory module, which stores the data at the appropriate address. When the access request is a read request, the memory controller 200 provides a read command and the address over the memory bus 310 to a memory module, which responds with the data from the memory location corresponding to the address within the memory module. The memory controller 200 may append a tag, and provides the data with the tag to the host bus 110. The central processing unit 100 thereupon recognizes the tag and receives the data from the host bus 110, and clears the tag for subsequent reuse")*

Claim 19. The system of claim 15, wherein the processor includes a page table cache having entries that include a field whose value is set by the processor in accordance with the first and second usage characteristics. *(Column 38, lines 20-23 – State the following: "Each of the memory access requests has, as a field thereof, an identifier that is unique among memory access requests pending on the host bus 110a")*

Claim 20. The system of claim 15, including a page table, for mapping virtual memory pages to physical memory pages, having a plurality of entries that include a field whose value is set in accordance with whether corresponding virtual memory pages are associated with the first or second usage characteristic. *(Column 19, lines 3-19 – State the following: "The sixth column of the table shown in Table 3, i.e., column 602A, shows the physical EDO DIMM 320, both size and type, that may be connected to the back end 306 of the memory personality module 300, assuming two physical EDO DIMMs are used for each logical memory module. Translation 690 proceeds as per Tables 7 and 9. For example, two 8-megabyte single row EDO DIMMs may be used at the back end of a*

*memory personality module 300 and mapped within the memory personality module to the front end and seen at the front end as a 16 megabyte single row SDRAM DIMM, as indicated in the first row of the table in Table 3. Alternatively, using smaller EDO DIMM physical memory modules, four physical EDO DIMM memory modules may be implemented as a singe logical EDO DIMM memory module 320, as shown in the seventh column of the table in Table 3, i.e., column 602B. Translation scheme 692' proceeds as per Tables 8 and 10")*

Claim 21. The system of claim 20, wherein the system is configured to change the value of the field in an entry of the page table based on usage of the corresponding page. *(Column 21, lines 59-67 and Column 22, lines 1-2 – State the following, which where frequency and usage are synonymous: "The memory personality module 300 also contain internal buffers for pending accesses, to reduce the frequency with which bus direction is reversed and thus maximize bandwidth on bus 310. Timing is managed by the memory controller 200 to accommodate read and write cycles as necessary to access the slowest physical memory module coupled to the memory personality module 300. Address and data bits may be posted in the memory personality module 300 pending write access to the memory bus 310. Posting allows the memory personality module 300 to reduce the latency of a write cycle")*

Claim 22. A method of managing memory in a non-homogeneous memory system, comprising: establishing a plurality of page table entries, each entry in the plurality of page table entries mapping a virtual memory page address to a physical memory page address, each said entry including a usage field identifying a respective portion of main memory in which the physical memory page address is located, wherein the main memory includes at least two distinct portions, including a first portion implemented with one or more first memory devices of a first memory type having a first set of attributes and a second portion implemented with one or more second

memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute; receiving a memory transaction request; translating a virtual address of a page associated with the memory transaction request into a physical address in accordance with a corresponding page table entry of the plurality of page table entries, the physical address comprising a physical address in a respective portion of main memory; directing the memory transaction to the physical address in the respective portion of main memory. *(Column 2, lines 32-46 – State the following: "Briefly, the present invention describes, in one embodiment, a memory controller capable of supporting heterogeneous memory configurations. Several different memory module types are coupled to a bus via the memory controller of the present invention, and communications occur seamlessly with the bus. The memory controller receives memory requests from one or more processors or other bus masters via the bus. The memory controller receives the memory request, identifies a memory, and also memory access parameters, and accesses the memory and returns the resulting data (during a read request) or stores the data (during a write request). When the memory provides the data (on a read request), to the memory controller, the memory controller provides the resulting data to the bus, where it can be read by the processor." Column 12, lines 30-38 – State the following: "The multiplexer or selector 720 is controlled by a control logic and controller 730. The control logic and controller 730 receives a system geographic address 732 and a serial clock 734, according to the I.sup.2 C protocol. The control logic and controller 730 provides a three bit selection signal over a selection bus 734 to the multiplexer and selector 720. The three bit selection signal cycles through the eight DIMMs 702-716, passing each of the parallel presence detect values 550 to the eight bit parallel presence detect bus 722 in turn." Column 25, lines 35-45 and Column 26, lines 1-3 and 23-45 – State the*

*following: "Referring now to Tables 4, 5, and 6, the internal bit mapping within the memory personality module 300, implementing some of the translations in Table 2 and Table 3, are shown in greater detail. The first column 572 shows possible SDRAM DIMM sizes used on bus 210. The front end 302 is coupled to memory bus 210 using a protocol according to column 572. The protocol according to column 572 is compatible with memory bus 210, memory module 240, and memory controller 200. The second column of Tables 4, 5, and 6., i.e., column 690, shows the bit mapping within the memory personality module 300 when the back end 306 is coupled to a logical DIMM consisting of two physical EDO DIMMs". "Address translation for multiple physical memory modules within a logical memory is further illustrated by way of an example. As shown in the first row of Tables 4, two 8-megabyte EDO DIMMs may be used at the back end 306 of the memory personality module 300, having 12 bits of row address and 8 bits of column address, as shown in column 690'. The front end 302 is connected to memory bus 210 requiring 11 bits of row address, 9 bits of column address, and one bank select bit BA0. During the bank activate command phase, the lower eleven bits of memory address on address bus 352 of the front end 302 are directly mapped to the lower eleven bits of memory address on memory address bus 362 at the back end 306. Also, the bank select bit BA0 at the front end 302 is mapped to the bit RA11 of memory address on memory address bus 362 at the back end 306. Subsequently, during the read or write command phase, the address bits A8 to A1 on address bus 352 at the front end 302 are mapped to the address bits A7 to A0 on memory address bus 362 at the back end 306, while address bits A1 and A0 are mapped as inputs to a chunk order control circuit to control the order in which the data chunks are to be bursted to/from memory")*

Claim 24. The method of claim 22, wherein the second memory devices are non-volatile memory devices and the first memory devices are volatile memory

devices. *(Column 12, lines 44-47 – State the following: "Both the high address on bus 722 and the low address on bus 736 are provided to a 32 KB ROM 740 or other memory such as Flash, embedded DRAM or SRAM, containing the corresponding look up table")*

Claim 26. The method of claim 22, wherein the second memory devices are non-volatile memory devices, and the method includes: redirecting at least one write operation directed to one of the second memory devices to a write cache. *(Column 4, lines 30-35 – State the following: "Also coupled to the host bus 110 is a cache 104. The cache may be a write through, a write back, or multi-level cache system for storing commonly used or recently used data values. The cache generally consists of a high-speed static RAM structure, addressable within the memory space of the processor's address lines")*

Claim 27. The method of claim 26, further comprising: determining if the write cache can accept a write operation; and writing the page to the write cache if the write cache can accept a write operation. *(Column 25, lines 9-13 – State the following: "The chunk order logic in the RPM is used to determine the order in which a 8-byte wide chunk of data (within a 32-byte or 64-byte wide cache line) is transferred onto memory data bus 370 on bus 310 when data is accessed over the memory bus 310")*

Claim 30. The method of claim 22, including moving pages from the one or more first memory devices to secondary storage and then powering down the one or more first memory devices. *(Column 25, lines 9-13 – State the following: "The chunk order logic in the RPM is used to determine the order in which a 8-byte wide chunk of data (within a 32-byte or 64-byte wide cache line) is transferred onto memory data bus 370 on bus 310 when data is accessed over the memory bus 310")*

Claim 31. A controller, comprising: first interface means for coupling the controller to one or more first memory devices of a first memory type having a first set of attributes; second interface means for coupling the controller to one

or more second memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute; and logic means coupled to the first and second interface means for directing memory transactions having a predefined first characteristic to the first memory interface and for directing memory transactions having a predefined second characteristic to the second memory interface. *(Column 2, lines 32-46 – State the following: "Briefly, the present invention describes, in one embodiment, a memory controller capable of supporting heterogeneous memory configurations. Several different memory module types are coupled to a bus via the memory controller of the present invention, and communications occur seamlessly with the bus. The memory controller receives memory requests from one or more processors or other bus masters via the bus. The memory controller receives the memory request, identifies a memory, and also memory access parameters, and accesses the memory and returns the resulting data (during a read request) or stores the data (during a write request). When the memory provides the data (on a read request), to the memory controller, the memory controller provides the resulting data to the bus, where it can be read by the processor." Column 12, lines 30-38 – State the following: "The multiplexer or selector 720 is controlled by a control logic and controller 730. The control logic and controller 730 receives a system geographic address 732 and a serial clock 734, according to the I.sup.2 C protocol. The control logic and controller 730 provides a three bit selection signal over a selection bus 734 to the multiplexer and selector 720. The three bit selection signal cycles through the eight DIMMs 702-716, passing each of the parallel presence detect values 550 to the eight bit parallel presence detect bus 722 in turn." Column 25, lines 35-45 and Column 26, lines 1-3 and 23-45 – State the following: "Referring now to Tables 4, 5, and 6, the internal bit mapping within the memory personality module 300,*

*implementing some of the translations in Table 2 and Table 3, are shown in greater detail. The first column 572 shows possible SDRAM DIMM sizes used on bus 210. The front end 302 is coupled to memory bus 210 using a protocol according to column 572. The protocol according to column 572 is compatible with memory bus 210, memory module 240, and memory controller 200. The second column of Tables 4, 5, and 6., i.e., column 690, shows the bit mapping within the memory personality module 300 when the back end 306 is coupled to a logical DIMM consisting of two physical EDO DIMMs". "Address translation for multiple physical memory modules within a logical memory is further illustrated by way of an example. As shown in the first row of Tables 4, two 8-megabyte EDO DIMMs may be used at the back end 306 of the memory personality module 300, having 12 bits of row address and 8 bits of column address, as shown in column 690'. The front end 302 is connected to memory bus 210 requiring 11 bits of row address, 9 bits of column address, and one bank select bit BA0. During the bank activate command phase, the lower eleven bits of memory address on address bus 352 of the front end 302 are directly mapped to the lower eleven bits of memory address on memory address bus 362 at the back end 306. Also, the bank select bit BA0 at the front end 302 is mapped to the bit RA11 of memory address on memory address bus 362 at the back end 306. Subsequently, during the read or write command phase, the address bits A8 to A1 on address bus 352 at the front end 302 are mapped to the address bits A7 to A0 on memory address bus 362 at the back end 306, while address bits A1 and A0 are mapped as inputs to a chunk order control circuit to control the order in which the data chunks are to be bursted to/from memory")*

Claim 32. The system, comprising: first interface means for coupling to one or more first memory devices of a first memory type having a first set of attributes; second interface means for coupling to one or more second memory devices of a second memory type having a second set of attributes,

wherein the first and second sets of attributes have at least one differing attribute; logic means coupled to the first and second interface means for directing memory transactions having a predefined first characteristic to the first memory interface and to direct memory transactions having a predefined second characteristic to the second memory interface; and virtual memory means for mapping virtual memory addresses into physical memory addresses and page means for assigning physical memory addresses to virtual memory addresses, wherein the page means assigned physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and assigns physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic. *(Column 2, lines 32-46 – State the following: "Briefly, the present invention describes, in one embodiment, a memory controller capable of supporting heterogeneous memory configurations. Several different memory module types are coupled to a bus via the memory controller of the present invention, and communications occur seamlessly with the bus. The memory controller receives memory requests from one or more processors or other bus masters via the bus. The memory controller receives the memory request, identifies a memory, and also memory access parameters, and accesses the memory and returns the resulting data (during a read request) or stores the data (during a write request). When the memory provides the data (on a read request), to the memory controller, the memory controller provides the resulting data to the bus, where it can be read by the processor." Column 12, lines 30-38 – State the following: "The multiplexer or selector 720 is controlled by a control logic and controller 730. The control logic and controller 730 receives a system geographic address 732 and a serial clock 734, according to the I.sup.2 C protocol. The control logic and controller 730 provides a three bit selection signal over a selection bus 734 to the*

*multiplexer and selector 720. The three bit selection signal cycles through the eight DIMMs 702-716, passing each of the parallel presence detect values 550 to the eight bit parallel presence detect bus 722 in turn."*
*Column 25, lines 35-45 and Column 26, lines 1-3 and 23-45 – State the following: "Referring now to Tables 4, 5, and 6, the internal bit mapping within the memory personality module 300, implementing some of the translations in Table 2 and Table 3, are shown in greater detail. The first column 572 shows possible SDRAM DIMM sizes used on bus 210. The front end 302 is coupled to memory bus 210 using a protocol according to column 572. The protocol according to column 572 is compatible with memory bus 210, memory module 240, and memory controller 200. The second column of Tables 4, 5, and 6., i.e., column 690, shows the bit mapping within the memory personality module 300 when the back end 306 is coupled to a logical DIMM consisting of two physical EDO DIMMs". "Address translation for multiple physical memory modules within a logical memory is further illustrated by way of an example. As shown in the first row of Tables 4, two 8-megabyte EDO DIMMs may be used at the back end 306 of the memory personality module 300, having 12 bits of row address and 8 bits of column address, as shown in column 690'. The front end 302 is connected to memory bus 210 requiring 11 bits of row address, 9 bits of column address, and one bank select bit BA0. During the bank activate command phase, the lower eleven bits of memory address on address bus 352 of the front end 302 are directly mapped to the lower eleven bits of memory address on memory address bus 362 at the back end 306. Also, the bank select bit BA0 at the front end 302 is mapped to the bit RA11 of memory address on memory address bus 362 at the back end 306. Subsequently, during the read or write command phase, the address bits A8 to A1 on address bus 352 at the front end 302 are mapped to the address bits A7 to A0 on memory address bus 362 at the back end 306, while address bits A1 and A0 are mapped as inputs to a*

*chunk order control circuit to control the order in which the data chunks are to be bursted to/from memory")*

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3 and 23 are rejected under 35 U.S.C.103(a) as being unpatentable over Olarig et al. as applied to claims 1-2 and 22, above, further in view of Sinclair (US Patent 6,578,127 B1).

Olarig teaches the limitations of claims 1-2 and 22 for the reasons above.

Olarig's invention differs from the claimed invention in that there is no specific reference to write operation endurance.

Olarig fails to teach claims 3 and 23, which respectively state "The controller of clam 2, wherein the second memory devices have a limited write operation endurance", and "The method of claim 22, wherein the first set of attributes include an unlimited endurance characteristic and the second set of attributes include a limited endurance characteristic". However, Sinclair's invention discloses the following: "However storage of control information is a problem for non-byte erasable memory because the information must be in a physical location which can be located by the control system after electrical power has been removed and then restored. Control information cannot be updated in a fixed physical location without bulk erasure of the memory medium but the number of erase/write cycles which can be applied to control information at a fixed physical location is restricted by the limited endurance

characteristics of the technology. The limited write/erase cycle endurance of FLASH EPROM technology is particularly acute" (Column 2, lines 15-25). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Method and Apparatus for Supporting Heterogeneous Memory in Computer Systems" of Olarig and Sinclair's "Memory Devices" before him at the time the invention was made, to make use write operation endurance so that there would be a clear measure of the write cycles that can be performed, which will enhance system efficiency.

4. Claims 4-5 and 25 are rejected under 35 U.S.C.103(a) as being unpatentable over Olarig et al. as applied to claims 1-3 and 22 above, further in view of Sinclair (US Patent 6,578,127 B1).

Olarig teaches the limitations of claims 1-3 and 22 for the reasons above.

Olarig's invention differs from the claimed invention in that there is no specific reference to counting the number of write cycles or having an endurance limitation.

Olarig fails to teach claims 4-5 and 25, which respectively state "The controller of claim 3, further comprising: an endurance counter for counting the number of write operations to a block of memory cells in the one or more second memory devices", and "The controller of claim 3, further comprising: a set of endurance counters for counting the number of write operations to each block of memory cells in the one or more second memory devices", "The method of claim 22, further comprising: determining if an endurance limitation associated with one of the second memory devices has been exceeded; and redirecting the memory transaction if the endurance limitation not been exceeded". However, Sinclair's invention discloses the following: "Included in this information is an erase counter to ensure that the physical limit for a block is not

exceeded" (Column 1, lines 24-26). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Method and Apparatus for Supporting Heterogeneous Memory in Computer Systems" of Olarig and Sinclair's "Memory Devices" before him at the time the invention was made, to include counting the number of write cycles and having an endurance limitation so that there would be a clear measure of the write cycles that can be performed, which will enhance system efficiency.

5. Claims 11-12 and 28-29 are rejected under 35 U.S.C.103(a) as being unpatentable over Olarig et al. as applied to claims 1 and 22 above, further in view of Coldewey (US PG Pub 2004/0133747 A1).

Olarig teaches the limitations of claims 1 and 22 for the reasons above.

Olarig's invention differs from the claimed invention in that there is no specific reference to a prefetch buffer.

Olarig fails to teach claims 11-12 and 28-29, which respectively state "The controller of claim 1, further comprising: a prefetch buffer coupled to the second interface and adapted to prefetch data from the one or more second memory devices", "The controller of claim 11, wherein the second interface is configured to reduce power used by the one or more second memory devices between prefetches of data from the one or more second memory devices", "The method of claim 22, wherein the second memory devices are non-volatile memory devices and the method includes: pre-fetching data from the second memory device", and "The method of claim 28, including reducing power to the one or more second memory devices between prefetches". However, Coldewey's invention discloses the following: "The general structure of the accumulation process is illustrated in FIG. 8. A search request consists of a transaction

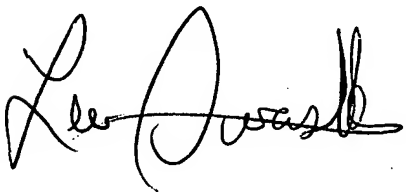
descriptor <k,r,a.sub.i>, where k is the search key associated with the request data structure identifier r, and a.sub.i is the initial prefetch target address, such as the address of the root node of a search tree or the initial hash bucket in the bucket chain of a hash table. One or more prefetch descriptors are associated with each data structure. A prefetch descriptor stores the invariants among accumulated requests, characterizing the prefetch target by the pipeline depth D, the startup threshold K, the completion threshold Z, the number of bytes to prefetch at each request, and a small buffer for several words of application-defined data. [0033] Search requests are accumulated in AQ, the accumulation queue. When the number of elements in the queue reaches the startup threshold, K, then D search requests are dequeued from the accumulation queue. The address portion of each request is submitted to the prefetch hardware along with the prefetch parameters from the prefetch descriptor, and the request is enqueued on the prefetch issued queue. This sequence of actions corresponds to the prologue of software-controlled prefetching" (Sections 0032-0033). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Method and Apparatus for Supporting Heterogeneous Memory in Computer Systems" of Olarig and Coldewey's "Method and Apparatus for Prefetching Recursive Data Structures" before him at the time the invention was made, to include a prefetch buffer so that the system would be able to predict operations and would therefore run in a more efficient manner.

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658 and fax number is (571)273-1658. The examiner can normally be reached on M-Th, from 8-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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